Dr. Osama O. Awadelkarim

Professor of Engineering Science and Mechanics

Office phone: (814) 863-1773
Office address: 407D EES BL
E-mail: ooaesm@engr.psu.edu

Current Events

- In the News

Degrees

- B.Sc (Honors), Physics - Khartoum University, 1977
- Ph.D., Physics - Reading University (United Kingdom), 1982

General

- Number of Years Service on this Faculty
  - Apr 1992 - Dec 1993, Research Associate
  - Jan 1994 - Jun 1994, Senior Research Associate
  - Jul 1994 - Jun 2000, Associate Professor of Engineering Science and Mechanics
  - Jul 2000 - Present, Professor of Engineering Science and Mechanics

- Other Related Experience - Teaching, Industrial, etc.
  - Jan 1982 - Jan 1987, Assistant Professor, Department of Physics, University of Khartoum, Khartoum, Sudan
  - Jan 1987 - Jan 1992, Research Scientist, Linkoping University & Swedish Defense Research Establishment, Linkoping, Sweden
  - Jan 1987 - Jan 1992, Research Scientist, Swedish Defense Research Establishment, Linkoping, Sweden

Research Interests

1. Power Electronics and Vertical U-Shaped Trench-Gated Metal-Oxide-Silicon Field-Effect Transistors Fairchild Semiconductor, Inc. Research in this area is in progress since 1999 and is conducted in collaboration with Fairchild Semiconductor, Inc. The goal is to develop and characterize a trench (~ 400 nm wide and 2.0 microns deep) structure for use in discrete power U-MOSFET device manufacturing. The focus of the research is on the following main tasks.

- Optimization of the trench etch conditions, trench side-wall cleaning, and oxide growth conditions.
- Development of models and tests allowing prediction of reliability of thick (>50 nm) gate oxides. As a part of this effort attempts are made to identify origins of fragility on the charge-to-breakdown of gate oxides in trenches. Also hot carrier stress reliability of the devices is assessed.
- Study of the damage occurring near to the drain edge of the U-MOSFET. This study is carried out using special structures that amplify the trench corner effects. More detailed transistor analysis and capacitance-voltage measurements on single and multiple U-MOSFET structures and trench capacitors are in progress.
- Investigate lower temperatures of oxidation, and thinner gate oxides (~10 nm) needed in devices for low-voltage logic and p-channel device applications.

2. Nanoelectronics and Complementary Metal-Oxide-Silicon (CMOS)/Integrated Circuit (IC) Processing: Ultra-Thin Gate Oxides and High-k Gate Dielectrics This research is concerned with the development of a gate stack system (dielectric, electrode, and their compatibility with plasma etching processes and the scaled complementary metal oxide semiconductor [CMOS] integrated circuit [IC] process flow). This issue presents major materials and processing

challenges as IC industry approaches the sub-100 nm technology generation by the year 2006 and beyond. The two main research thrusts are :

- Thin gate-oxides (SiO_2 of thickness below 5 nm) metal-oxide-Si (MOS) capacitor and MOS field-effect transistor (MOSFET) structures are fabricated using submicron full CMOS process flow. Damage to these structures caused by different processing steps, is studied using transistor parameter measurements, charge pumping, as well as deep-level transient spectroscopy (DLTS). Device reliability is also assessed using appropriately developed Fowler-Nordheim (FN) and hot carrier (HC) stressing protocols.

- Different high-k dielectrics, such as TiO_2, $SrTa_2O_6$, $ZrSiO_4$, and HfO_2 are prepared by a variety of thin film deposition techniques. These include liquid source misted chemical deposition and chemical vapor deposition. Following deposition, detailed investigations of the electrical properties and reliabilities of these dielectrics and their interfaces with Si are carried out. As test vehicles these investigations employ metal-insulator-Si (MIS) capacitors and MISFETs devices, where the high-k dielectric is used as the gate insulator.

3. Nanoelectronics and Complementary Metal-Oxide-Silicon (CMOS)/Integrated Circuit (IC) Processing: Low-k Inter-Layer Dielectrics (ILDs) for Ultra Large-Scale Integration (ULSI) In this research area new low-k materials for ILD applications in ULSI are prepared and examined in terms of their physical and chemical properties as well as their compatibility with integrated circuit technologies. The low-k materials examined include fluorinated silicon oxides, polymers, and sculptured silicon oxides.

4. Microsensors and MEMS The ongoing research in this area is carried out in collaboration with Fairchild Semiconductors Inc. The current focus is in thermal microsensors in the form of a single p/n junction diode and arrays of several stack diodes. The properties and output of

the microsensor are examined as functions of junction dimensions and scaling, temperature range, and reverse breakdown characteristics.

5. Thin-Film Transistors (TFTs) for Display and Microsensor Applications This is a study of the characteristics of polycrystalline silicon/polymer TFTs fabricated on various rigid or flexible substrates. These may be bare substrates or substrates coated with different semiconducting/insulating films. The study addresses issues regarding the performance and stability of the TFTs as function of polycrystalline silicon/polymer film preparation (deposition methods and conditions, annealing, etc.), coating material type and thickness, and substrate materials

Publications

Principal Publications of Last Five Years (partial list)

1. “A study of carrier-trap generation by Fowler-Nordheim tunneling stress on polycrystalline-silicon/ SiO2/ silicon structures”, J. Jiang, O.O. Awadelkarim, and Y.D. Chan: Solid-State Electonics, 41(1), 41-46 (1997).
2. “The impact of metal-1 plasma processing-induced hot carrier injection on the characteristics and reliability of n-MOSFETs”, M.G. ElHassan, O.O. Awadelkarim, and J. Werking: IEEE Transactions on Electronic Devices, 45(4), 861-866 (1998).
3. “The dependence of the performance and reliability of n-MOSFETs on interlayer dielectric processing,L. Trabzon”, O.O. Awadelkarim, and J. Werking: J. Vacuum Science and Technology B1, 7(5), 2216-2221 (1999).
4. “The impact of trench geometry and processing on the performance and reliability of low voltage power UMOSFETs”, S.A. Suliman, N. Gollagunta, L. Trabzon, J. Hao, G. Dolny, R. Ridley, T. Grebs, J. Benjamin, C. Kocon, J. Zeng, C.M. Knoedler, M. Horn, O.O. Awadelkarim, S.J. Fonash, and J. Ruzyllo: Proceedings of the 39th International Reliability Physics

Symposium, Sponsored by IEEE Electron Devices Society and IEEE Reliability Society, Orlando, FL, April 30th–May 3rd, 308-314 (2001).
5. "The dependence of UMOSFET characteristics and reliability on geometry and processing", S.A. Suliman, N. Gollagunta, L. Trabzon, J. Hao, R.S. Ridley, C.M. Knoedler, G.M. Dolny, O.O. Awadelkarim, and S.J. Fonash: Semicond. Sci. Technol. 16, 447-454 (2001).
6. "Characterization of gate oxide degradation mechanisms in trench-gated power MOSFETs using the charge pumping technique", G. Dolny, N. Gollagunta, S.A. Suliman, L. Trabzon, M. Horn, O.O. Awadelkarim, S.J. Fonash, J. Hao, R.S. Ridley, T. Grebs, J. Zeng, and C. Kocon: Proceeding of 2001 International Symposium on Power Semiconductor Devices & ICs, ISPSD, 431-434 (2001).
7. "The effects of channel boron doping on the performance and hot electron reliability of n-channel trench UMOSFETs", S.A. Suliman, O.O. Awadelkarim, S.J. Fonash, G.M. Dolny, J. Hao, R.S. Ridley, and C.M. Knoedler: Solid-State Electronics, 45, 655-661 (2001).
8. "The degradation of MOSFETs induced by the via etching of interlayer low-k polymers", L. Trabzon and O.O. Awadelkarim: Proceedings of the 13th IEEE International Conference on Microelectronics (IMC), Rabat, Morocco, Oct. 29-31, 103-106, (2001).
9. "Electron and hole trapping in the bulk and interface with Si of a thermal oxide grown on the sidewalls and base of a U-shaped silicon trench", S.A. Suliman, O.O. Awadelkarim, S.J. Fonash, R.S. Ridley, G.M. Dolny, J. Hao, and C. M. Knoedler: Solid-State Electronics, 46(6), 837-845 (2002).
10. "On the capacitance of metal/high-k dielectric material stack/silicon structures", J. Jian, O.O. Awadelkarim, D-O Lee, P. Roman and J. Ruzyllo: Solid State Electronics, 46, 1991-1995 (2002).
11. "Growth and reliability of thick gate oxide in U-trench for power MOSFETs", C.T. Wu, R.S. Ridley, G. Dolny, T. Grebs, C.

Knoedler, S.A. Suliman, B. Venkataraman, O.O. Awadelkarim and J. Ruzyllo: Proceeding of 2002 14th International Symposium on Power Semiconductor Devices & ICs, ISPSD, 149-152 (2002).

12. "The utilization and effects of plasma exposure on materials properties of low-k polymers in microelectronics", L. Trabzon and O.O. Awadelkarim: Proceedings of the 6th Biennial Conference on Engineering Systems Design and Analysis ESDA2002, Istanbul, Turkey, July 8-11 (2002).

Books

1. Proceedings of the Symposium on Giga Scale Integration Technology of the 35th Annual Technical Meeting of the Society of Engineering Science. Edited by M. A. Osman and O. O. Awadelkarim, held on September 27 - 30, 1998, Pullman, WA. (1999).
2. Microsensors, MEMS, and Smart Devices, Julian W. Gardner, Vijay K. Varadan, and Osama O. Awadelkarim, John Wiley & Sons, Ltd. (2001

Consultings

1. S. J. Fonash, O. O. Awadelkarim, M. Okandan, and M. Ozaita-Mintegui, Co-Inventors. "A novel technique for monitoring processing induced damage", PSU Inv. Disc. Nos. 96-1569 and 96-1602.
2. Consultant with SEMATECH, Austin, TX.

Memberships

1. Electrochemical Society
2. Material Research Society
3. International Society of Optical Engineering
4. American Society for Engineering Education

Awards

1. Shell Prize, University of Khartoum, Sudan, 1974.
2. University Prize (Best Graduating Student in Science), University of Khartoum, 1977.
3. Governmental Study Abroad Fellowship, 1977 to 1982, Government of Sudan.
4. Fellowships of the International Seminars in Physics and Chemistry, University of Uppsala (Sweden), 1984 and 1985

Services

1. Reviewer for the Journal of Electrochemical Society, since 1991
2. Reviewer for IEEE Transactions on Components, Packaging and Manufacturing Technology, since 1996
3. Reviewer for NSF, since 1996
4. Reviewer for SPIE Smart Materials and Structures, since 1996
5. Minority Engineering Program, Participant, 1996 - Present
6. Penn State Minority Engineering Program (MEP); fall 1996 - present.
7. Reviewer for Diamond and Related Materials, since 1997
8. Reviewer for IEEE Transactions on Electron Devices, since 1997
9. PSU Forum on Black Affairs, Committee Member, October 1997 - 1998
10. Contributed to developing a Memorandum of Understanding (MOU) in research and education with The Kharkiv State Polytechnic University (Ukraine) and ESM department, 1997 - 1998; contributing to on-going efforts to develop a MOU with Politecnico Di Milano (Italy) with ESM and AE; contributing to on-going efforts to develop a MOU with University of Linkoping (Sweden) and the University of Japan–both with ESM Department, 1997 - 1999
11. Member of program committees for SPIE Conference on “Smart Electronics and MEMS” for the years 1997, 1998, and 1999.

12. Member, Program Committee, Symposium on Giga Scale Integration Technology in the 35th Annual Technical Meeting of the Society for Engineering Science, Pullman, Washington, September, 1998
13. Member, Gate Stack Engineering Working Group, April 1998-present.
14. Research collaboration, Fairchild Semiconductor, Inc., Power MOSFETs Division, February 1999-present.
15. Member of the PSU Advisory Committee on International Students and Scholars (ACISS) 2000 - Present
16. Member of EPRI/ARPA sponsored industry-university team for flat panel display technologies; July - Present.
17. Reviewer for IEEE Electron Device Letters, since 2000
18. Member, Program committee, International Reliability Physics Symposium, Orlando, Fl, April 2001
19. Member, Program committee, International Reliability Physics Symposium (IRPS), 2001
20. Reviewer for J. Physics D, 2002
21. Reviewer for Nanotechnology Journal, 2002
22. Member, Review panel for NSF Graduate Research Fellowship Program (GRFP), February 2002.
23. Member, Review Panel for NSF Small Business Innovation Research (SBIR) evaluations panelist, April 2002.

Professional Development

1. Active in establishing contacts with Historically Black Colleges and Universities to promote afro-american undergraduate students in engineering research at Penn State, 1996 - Present.
2. Instructed a course in “Semiconductor Devices” broadcast live via interactive compressed video (ICV) conferenging to engineers in Lucent Technologies, Reading, PA.
3. Spring Semester 2001, EMch 12 (Dynamics); Spring Semester 2001 and 2002, EMch 481/581 (MEMS/MEMS and Smart Structures); Fall Semester 2001 and Spring Semester 2002 (EMch

13 (Strength of Materials): extensive utilization of the World-Wide-Web in the course material preparation, homework assignments and solutions, midterm exam preparations, solved problems and additional practice problems, and communicating information to students.